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EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,702	WILLIAMS, ROBERT ALAN	
	Examiner	Art Unit	
	Jason E Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 and 6-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kalkunte et al. (U.S. Pat. 6813268).

With respect to claim 1, Kalkunte et al. discloses a network device configured to control communication of data frames between stations **(See column 4 lines 12-47 and Figure 1 of Kalkunte et al. for reference to switch-on-chip (SOC) 10, which is a network device controlling the communication of frames between stations connected to ports)**. Kalkunte et al. also discloses a plurality of receive ports configured to receive data frames from the stations **(See column 4 lines 12-47 and Figure 1 of Kalkunte et al. for reference to fast Ethernet ports 13 and Ethernet ports 15 connected to the SOC 10)**. Kalkunte et al. further discloses a memory configured to store address information and data forwarding information **(See column 4 line 57 to column 5 line 19 and Figure 2 of Kalkunte et al. for reference to address**

resolution logic and layer 3 switching tables 21a, 21b, 21c, 31a, and 31b, which are memories configured to store address information and data forwarding information). Kalkunte et al. also discloses the address information and data forwarding information being stored as a plurality of entries in a first address table **(See Figures 27A-D of Kalkunte et al. for reference to address information and data forwarding information being stored as entries in tables)**. Kalkunte et al. further discloses a timer configured to transmit a signal at a predetermined interval of time defining an aging cycle associated with the first address table **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to an age timer that expires at a predetermined interval and initiates an aging process in ARL table 21 of a first SOC 10)**. Kalkunte et al. also discloses an aging device configured to receive the signal from the timer and initiate an aging process on the first table **(See column 22 line 65 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to EPIC module 20, with SOC 10, performing an aging process on ARL table 21 when the age timer sends a signal indicating it has expired)**. Kalkunte et al. further discloses interrupt logic configured to receive the signal from the timer and transmit an interrupt signal to an external device indicating that the aging process on the first address table has been initiated **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to after the timer has initiated the aging process on the first SOC 10, and when it is determined that an ALR entry is to be deleted, sending a delete ARL entry message, which indicates that an aging process has been initiated at the first SOC 10, on a shared CPS channel to other modules,**

which includes a second externally connected SOC 10 and an externally connected CPU 52).

With respect to claim 2, Kalkunte et al. discloses that the external device storing a second address table corresponding to the first address table stored in the memory of the network device **(See column 22 lines 33-64 for reference to the external device being a second externally connected SOC 10 that also includes an ARL/L3 table that is to be synchronized to the ARL table 21 of the first SOC 10)**. Kalkunte et al. also discloses the external device initiating an aging process on the second table **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to the first SOC 10 sending a delete ARL entry to the second externally connected SOC 10 on the CPS channel that the second externally connected SOC uses to initiate an aging process to delete to corresponding entry on in its own ARL table)**.

With respect to claim 3, Kalkunte et al. discloses that each entry in the first address table includes an address hit field and an aging override field **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to checking a to see if an address entry in the ARL table 21 has a hit bit set or if an entry is a static entry, meaning each table entry includes a hit address field and a static entry field, which is an aging override field)**. Kalkunte et al. also discloses examining each of the entries in the first address table and determining whether to at least one of delete and invalidate an entry based on the address hit field and aging override field **(See column 22 line 65 to column 23 line 29 and Figure 18 of Kalkunte et al. for**

reference to determining whether to delete and entry in the ALR 21 based on if the hit bit is set of if the entry is a static entry).

With respect to claim 4, Kalkunte et al. discloses a second externally connected SOC 10 that is connected to and synchronizes ALR tables with the first SOC 10 **(See column 22 lines 33-64 for reference to synchronizing ARL tables between multiple SOC 10)**. Since the externally connected device is the same type of device as the first SOC 10, the second device also contains a second ARL table with entries including a hit field and an aging override field as discussed above. Further, the second externally connected SOC 10 performs the same aging process to delete an entry based on the hit field and the aging override field as described above.

With respect to claim 6, Kalkunte et al. discloses that the aging process performed on the first address table is substantially synchronized with an aging process performed on a second address table stored in the external device **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference the first SOC 10 sending update messages to all externally connected devices each time a change is made in ARL table 21 so that the address tables of all the devices are substantially synchronized during the aging processes)**.

With respect to claim 7, Kalkunte et al. discloses that the aging device comprises an aging stat machine that performs a hardware-controlled aging process on the first address table **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to the EPIC module 20 including hardware to perform the aging process on the first ARL table 21 of the first SOC 10)**. Kalkunte et al. also discloses

that the external device comprises a processor and memory storing a second address table corresponding to the first address table and that the processor performs a software-controlled aging process on the second address table **(See column 11 line 51 to column 12 line 4 and column 22 lines 33-64 of Kalkunte et al. for reference to a CPU 52, which comprises a processor, also storing an address table that is updated using software so the address information in the CPU 52 is synchronized with the ARL table 21 of the first SOC 10 using an aging process)**.

With respect to claim 8, Kalkunte et al. discloses a method comprising storing information in a memory of a network device **(See column 4 line 57 to column 5 line 19 and Figure 2 of Kalkunte et al. for reference to address resolution logic and layer 3 switching tables 21a, 21b, 21c, 31a, and 31b, which are memories of a SOC 10 configured to store address information and data forwarding information)**. Kalkunte et al. also discloses information being stored as a plurality of entries including address information and forwarding information **(See Figures 27A-D of Kalkunte et al. for reference to address information and data forwarding information being stored as entries in tables)**. Kalkunte et al. further discloses receiving data frames on a plurality of receive ports of the network device **(See column 4 lines 12-47 and Figure 1 of Kalkunte et al. for reference to fast Ethernet ports 13 and Ethernet ports 15, where data frames are received from, connected to the SOC 10)**. Kalkunte et al. also disclose initiating an aging process on the first address table at predetermined intervals of time **(See column 22 line 65 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to initiating a aging process at predetermined**

intervals dictated by an age timer). Kalkunte et al. further discloses transmitting a signal to an external device at the predetermined intervals of time indicating that the aging process on the first address table has been initiated **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to after the timer has initiated the aging process on the first SOC 10, and when it is determined that an ALR entry is to be deleted, sending a delete ARL entry message, which indicates that an aging process has been initiated at the first SOC 10, on a shared CPS channel to other modules, which includes a second externally connected SOC 10 and an externally connected CPU 52)**.

With respect to claim 9, Kalkunte et al. discloses a second externally connected SOC 10 that is connected to and synchronizes ALR tables with the first SOC 10 **(See column 22 lines 33-64 for reference to synchronizing ARL tables between multiple SOC 10)**. Since the externally connected device is the same type of device as the first SOC 10, the second device also contains a second ARL table. Further, the second externally connected SOC 10 performs the same aging process as the first SOC 10 based on the delete ARL entry messages received from the first SOC 10 as described above.

With respect to claim 10, Kalkunte et al. discloses that the aging process performed on the first address table is substantially synchronized with an aging process performed on a second address table stored in the external device **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference the first SOC 10 sending update messages to all externally connected devices each time a**

change is made in ARL table 21 so that the address tables of all the devices are substantially synchronized during the aging processes).

With respect to claim 11, Kalkunte et al. discloses a second externally connected SOC 10 that is connected to and synchronizes ALR tables with the first SOC 10 **(See column 22 lines 33-64 for reference to synchronizing ARL tables between multiple SOC 10)**. Since the externally connected device is the same type of device as the first SOC 10, the second device also contains a second ARL table that is synchronized with the ALR table 21 of the first SOC 10 **(See column 22 lines 33-64 of Kalkunte et al. for reference to synchronizing ARL tables)**. Kalkunte et al. also discloses modifying the first address table based on the received data frames, monitoring by the external device the modifications to the first address table, and updating the second address table based on the modifications to the first address table **(See column 22 lines 33-64 of Kalkunte et al. for reference to the first SOC 10 updating its ARL table 21 based with a new source address, and for reference to the second externally connected SOC 10 monitoring S channel 83 for an ARL insert message and updating its corresponding ARL table based on the modification to the first ARL table 21)**.

With respect to claim 12, Kalkunte et al. disclose setting a hit bit in a first entry in the first address table when information included in a received data frame matches the information in the first entry **(See column 22 lines 33-64 of Kalkunte et al. for reference to setting a "hit bit" corresponding to received data frames matching table entries)**.

With respect to claim 13, Kalkunte et al. discloses that each entry in the first address table includes an address hit field and an aging override field **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to checking a to see if an address entry in the ARL table 21 has a hit bit set or if an entry is a static entry, meaning each table entry includes a hit address field and a static entry field, which is an aging override field)**. Kalkunte et al. also discloses reading each entry in the first address table and determining whether to at least one of delete and invalidate an entry based on the address hit field and aging override field **(See column 22 line 65 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to determining whether to delete and entry in the ALR 21 based on if the hit bit is set of if the entry is a static entry)**.

With respect to claim 14, Kalkunte et al. discloses a second externally connected SOC 10 that is connected to and synchronizes ALR tables with the first SOC 10 **(See column 22 lines 33-64 for reference to synchronizing ARL tables between multiple SOC 10)**. Since the externally connected device is the same type of device as the first SOC 10, the second device also contains a second ARL table with entries including a hit field and an aging override field as discussed above. Further, the second externally connected SOC 10 performs the same aging process to delete an entry based on the hit field and the aging override field as described above.

With respect to claim 15, Kalkunte et al. discloses a system comprising a network device configured to received data frames from a plurality of stations and generate frame forwarding information for the received data frames **(See column 4**

lines 12-47 and Figure 1 of Kalkunte et al. for reference to switch-on-chip (SOC) 10, which is a network device controlling the communication and forwarding of frames between stations connected to ports). Kalkunte et al. also discloses a first memory configured to store address information and data forwarding information **(See column 4 line 57 to column 5 line 19 and Figure 2 of Kalkunte et al. for reference to address resolution logic and layer 3 switching tables 21a, 21b, 21c, 31a, and 31b, which are memories configured to store address information and data forwarding information)**. Kalkunte et al. further discloses the address information and data forwarding information being stored as a plurality of entries in a first address table **(See Figures 27A-D of Kalkunte et al. for reference to address information and data forwarding information being stored as entries in tables)**. Kalkunte et al. also discloses a timer configured to transmit a time-out signal at predetermined intervals of time defining an aging cycle associated **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to an age timer that expires at a predetermined interval and initiates an aging process in ARL table 21 of a first SOC 10)**. Kalkunte et al. further discloses an aging mechanism configured to received the time-out signal and initiate an aging process on the first address table **(See column 22 line 65 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference to EPIC module 20, with SOC 10, performing an aging process on ARL table 21 when the age timer sends a signal indicating it has expired)**. Kalkunte et al. also discloses a logic device configured to receive the time-out signal and transmit an interrupt signal **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for**

reference to after the timer has initiated the aging process on the first SOC 10, and when it is determined that an ALR entry is to be deleted, sending a delete ARL entry message, which indicates that an aging process has been initiated at the first SOC 10, on a shared CPS channel to other modules, which includes a second externally connected SOC 10 and an externally connected CPU 52). Kalkunte et al. further discloses an external processing device comprising a second memory configured to store an address table, receive the interrupt signal, and initiate an aging process on the second address table **(See column 11 line 51 to column 12 line 4 and column 22 lines 33-64 of Kalkunte et al. for reference to a CPU 52, which comprises a processor, also storing an address table that is updated using software so the address information in the CPU 52 is synchronized with the ARL table 21 of the first SOC 10 using an aging process initiated by receiving the delete ARL entry message).**

With respect to claim 16, Kalkunte et al. discloses that the aging process performed on the first address table is substantially synchronized with an aging process performed on a second address table stored in the external device **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference the first SOC 10 sending update messages to all externally connected devices, including CPU 52, each time a change is made in ARL table 21 so that the address tables of all the devices are substantially synchronized during the aging processes).**

With respect to claim 17, Kalkunte et al. discloses that the aging device comprises an aging stat machine that performs a hardware-controlled aging process on

the first address table **(See column 22 line 65 to column 23 line 29 of Kalkunte et al. for reference to the EPIC module 20 including hardware to perform the aging process on the first ARL table 21 of the first SOC 10)**. Kalkunte et al. also discloses that the external device comprises a processor and memory storing a second address table corresponding to the first address table and that the processor performs a software-controlled aging process on the second address table **(See column 11 line 51 to column 12 line 4 and column 22 lines 33-64 of Kalkunte et al. for reference to a CPU 52, which comprises a processor, also storing an address table that is updated using software so the address information in the CPU 52 is synchronized with the ARL table 21 of the first SOC 10 using an aging process)**.

With respect to claim 18, Kalkunte et al. discloses that the aging mechanism and the logic device receive the time-out signal at substantially the same time **(See column 22 line 33 to column 23 line 29 and Figure 18 of Kalkunte et al. for reference the first SOC 10 sending update messages to all externally connected devices, including CPU 52, each time a change is made in ARL table 21 so that the address tables of all the devices are substantially synchronized during the aging processes, in response to the age timer timing out)**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kalkunte et al. in view of Szczepanek et al. (U.S. Publication US2003/0110344).

With respect to claim 5, Kalkunte et al. does not disclose that the timer is programmable.

Szczepanek et al., in the field of communications, discloses an aging timer that is programmable **(See page 6 paragraph 144 of Szczepanek et al. for reference to an aging time being programmable)**. A programmable aging time has the advantage of allowing the user of a switching device greater control over how often an address table is to be updated, so that depending on the environment in which the device is used, the timing of the aging process can be optimized.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Szczepanek et al., to combine the programmable aging timer of Szczepanek et al. with the network device of Kalkunte et al. with the motivation being to allow the user of a switching device greater control over how often an address table is to be updated, so that depending on the environment in which the device is used, the timing of the aging process can be optimized.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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